FIG.1

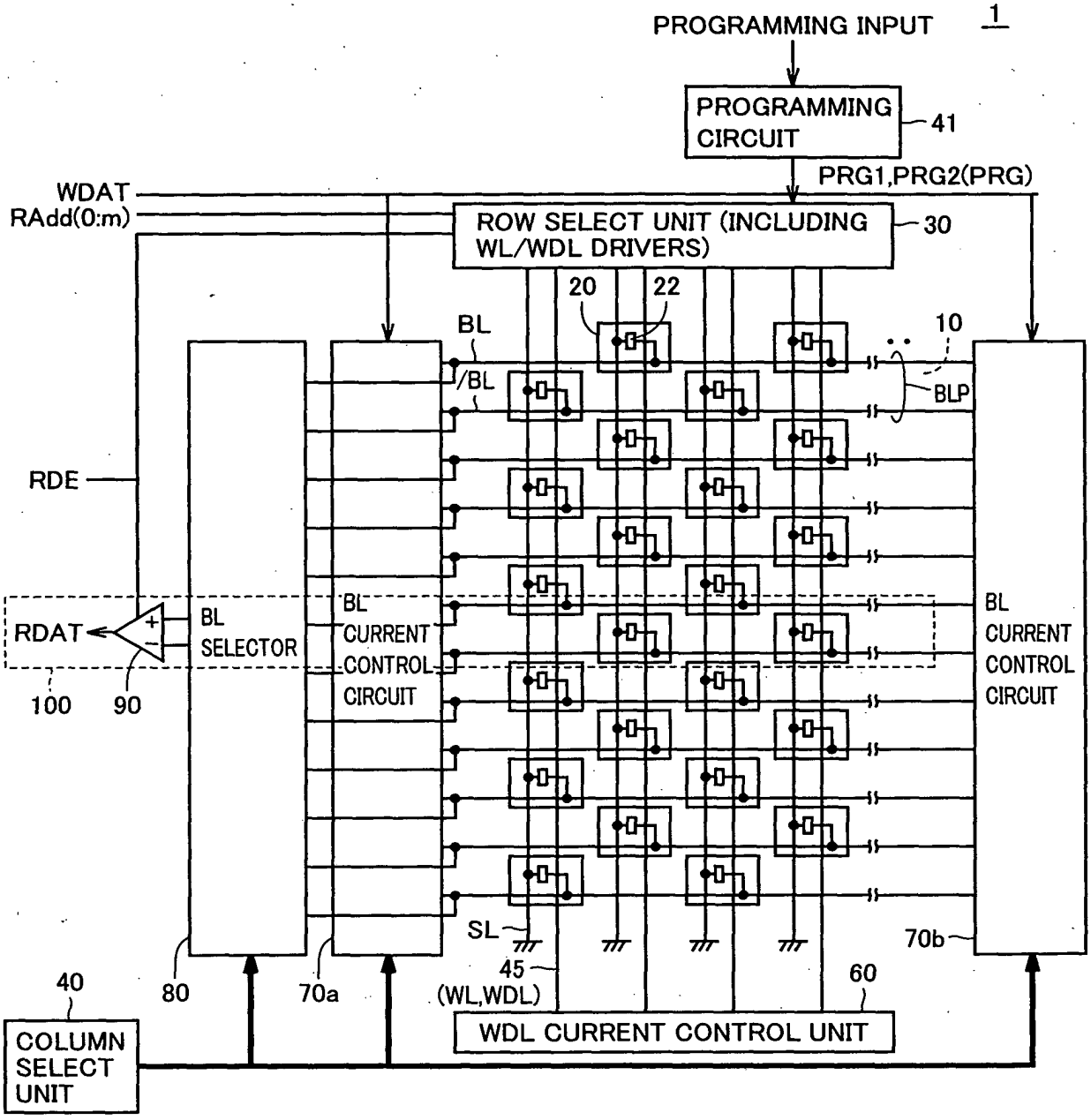

PROGRAMMING INPUT
1
PROGRAMMING CIRCUIT
41
PRG1,PRG2(PRG)
WDAT
RAdd(0:m)
ROW SELECT UNIT (INCLUDING WL/WDL DRIVERS)
30
20
22
BL
/BL
10
BLP
RDE
RDAT
BL SELECTOR
BL CURRENT CONTROL CIRCUIT
100
90
BL CURRENT CONTROL CIRCUIT
SL
70b
40
80
70a
45
(WL,WDL)
60
COLUMN SELECT UNIT
WDL CURRENT CONTROL UNIT

FIG.2

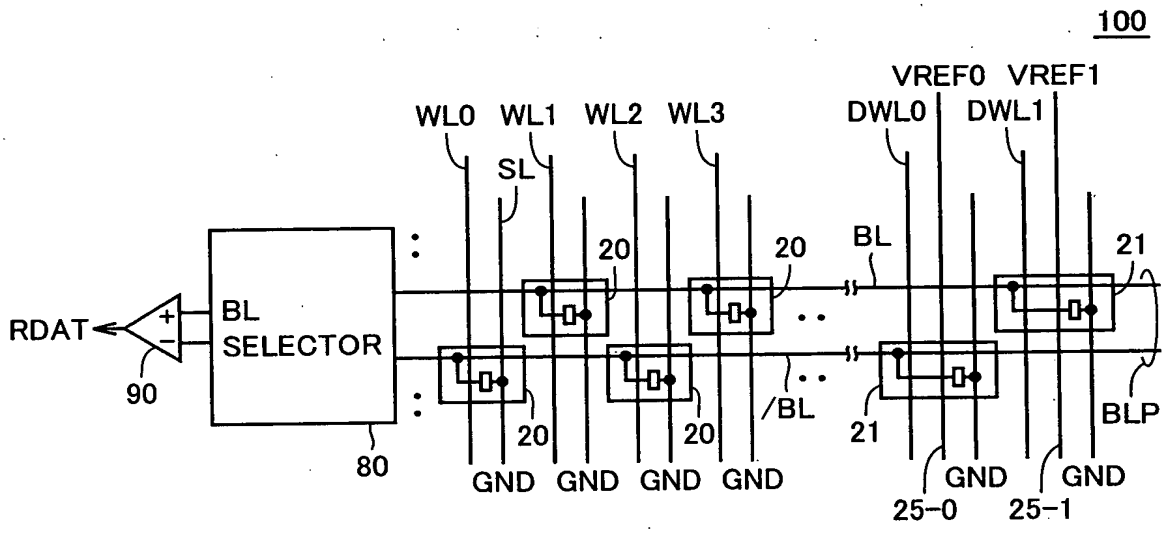

100
VREF0
VREF1
WL0
WL1
WL2
WL3
DWL0
DWL1
SL
BL
21
20
20
RDAT
BL
SELECTOR
90
80
/BL
BLP
GND
GND
GND
GND
GND
GND
25-0
25-1

FIG.3

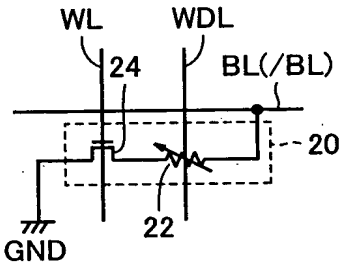

WL
WDL
24
BL(/BL)
20
22
GND

FIG.4

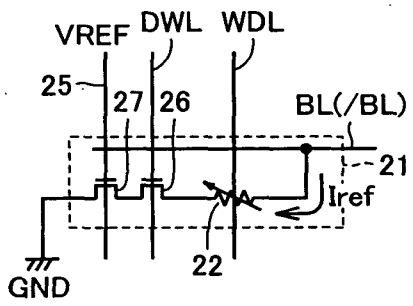

VREF
DWL
WDL
25
27
26
BL(/BL)
21
Iref
22
GND

FIG.5

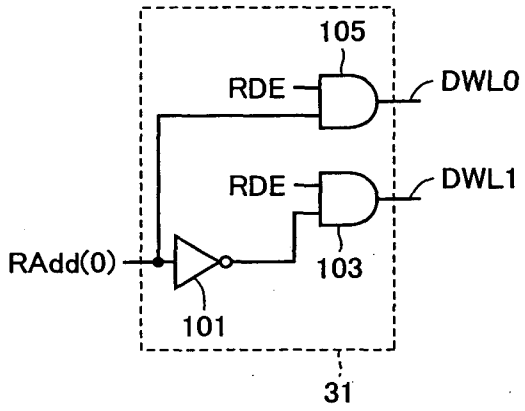

105
RDE
DWL0
RDE
DWL1
RAdd(0)
103
101
31

FIG.6

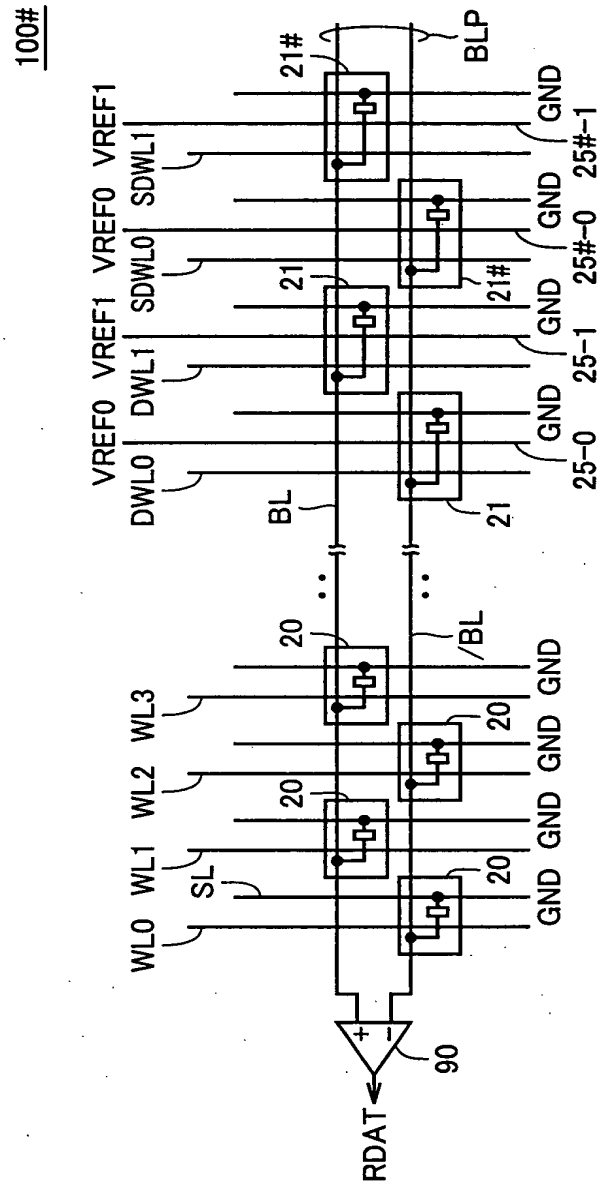

100#
VREF0 VREF1 VREF0 VREF1
DWL0 DWL1 SDWL0 SDWL1
WL0 WL1 WL2 WL3
SL
BL
/BL
BLP
21
21#
20
25-0
25-1
25#-0
25#-1
GND
90
RDAT

FIG.7

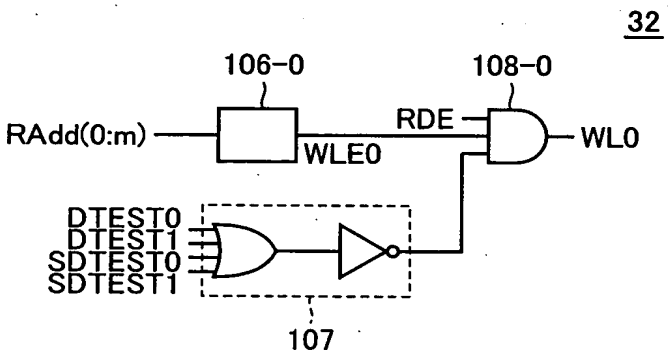


FIG.8

TEST CONTROL SIGNAL	TEST PATTERN i)	ii)	iii)	iv)
DTEST0	H	L	L	L
DTEST1	L	H	L	L
SDTEST0	L	L	H	L
SDTEST1	L	L	L	H

REFERENCE CELL TEST MODE

SPARE REFERENCE CELL TEST MODE

FIG.9

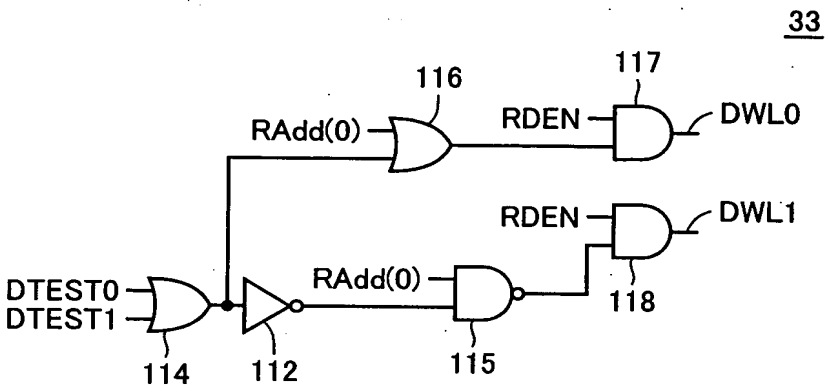

33
116
117
RAdd(0)
RDEN
DWL0
RDEN
DWL1
DTEST0
DTEST1
RAdd(0)
118
114
112
115

FIG.10

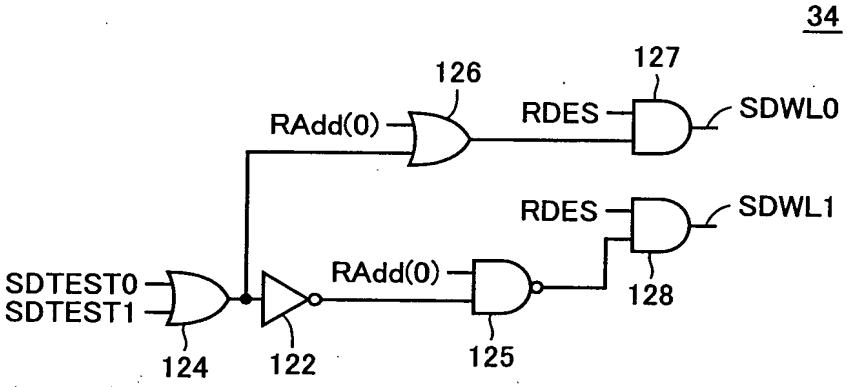

34
126
127
RAdd(0)
RDES
SDWL0
RDES
SDWL1
SDTEST0
SDTEST1
RAdd(0)
128
124
122
125

FIG.11

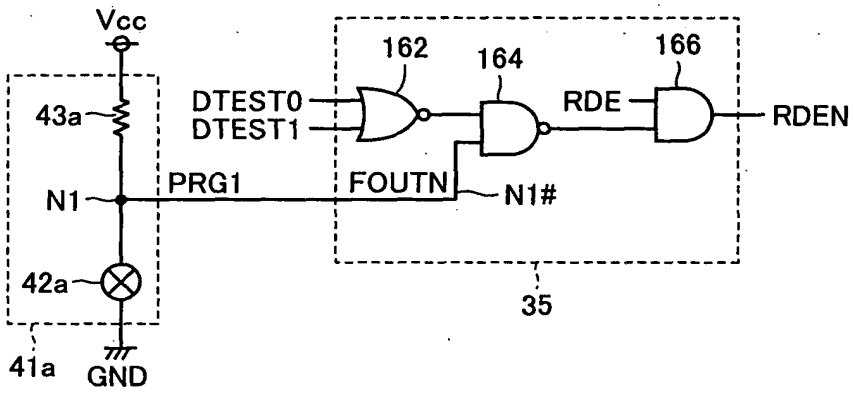

Vcc
43a
N1
42a
41a
GND
PRG1
DTEST0
DTEST1
162
164
166
RDE
RDEN
FOUTN
N1#
35

FIG.12

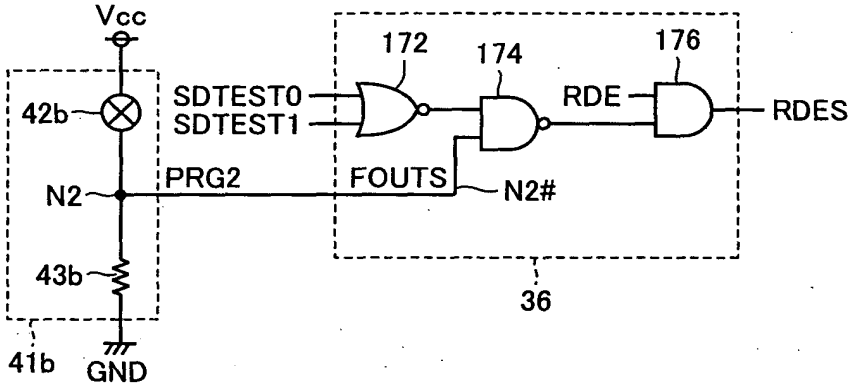

Vcc
42b
N2
43b
41b
GND
PRG2
SDTEST0
SDTEST1
172
174
176
RDE
RDES
FOUTS
N2#
36

FIG.13

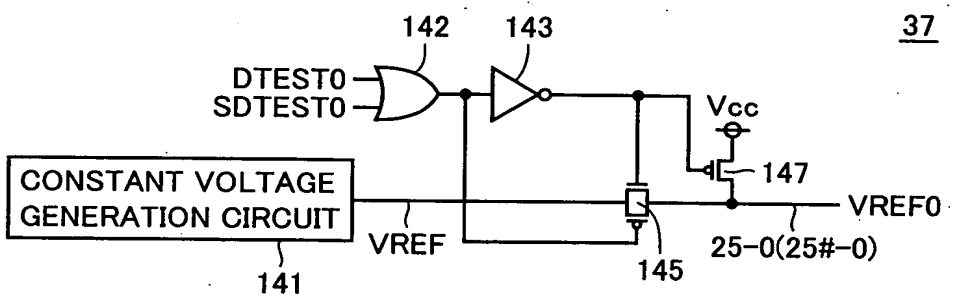

142
143
37
DTEST0
SDTEST0
Vcc
147
CONSTANT VOLTAGE GENERATION CIRCUIT
VREF0
VREF
25-0(25#-0)
145
141

FIG.14

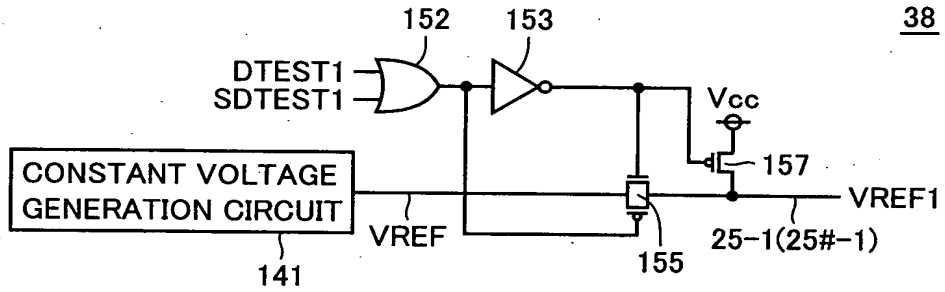

152
153
38
DTEST1
SDTEST1
Vcc
157
CONSTANT VOLTAGE GENERATION CIRCUIT
VREF1
VREF
25-1(25#-1)
155
141

FIG.15

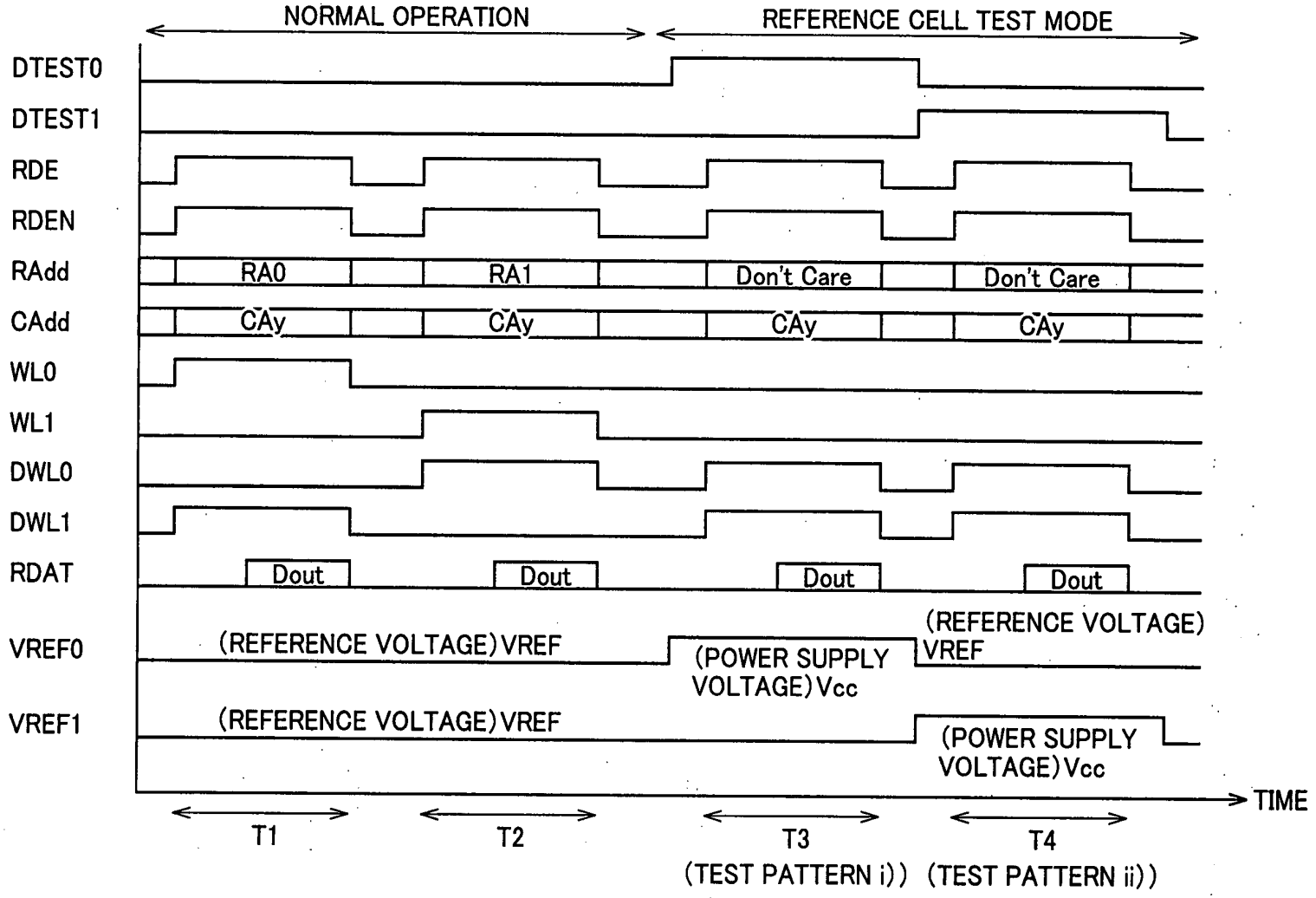

NORMAL OPERATION
REFERENCE CELL TEST MODE
DTEST0
DTEST1
RDE
RDEN
RAdd
RA0
RA1
Don't Care
Don't Care
CAdd
CAy
CAy
CAy
CAy
WL0
WL1
DWL0
DWL1
RDAT
Dout
Dout
Dout
Dout
VREF0
(REFERENCE VOLTAGE) VREF
(POWER SUPPLY VOLTAGE) Vcc
(REFERENCE VOLTAGE) VREF
VREF1
(REFERENCE VOLTAGE) VREF
(POWER SUPPLY VOLTAGE) Vcc
TIME
T1
T2
T3
T4
(TEST PATTERN i))
(TEST PATTERN ii))

FIG.16

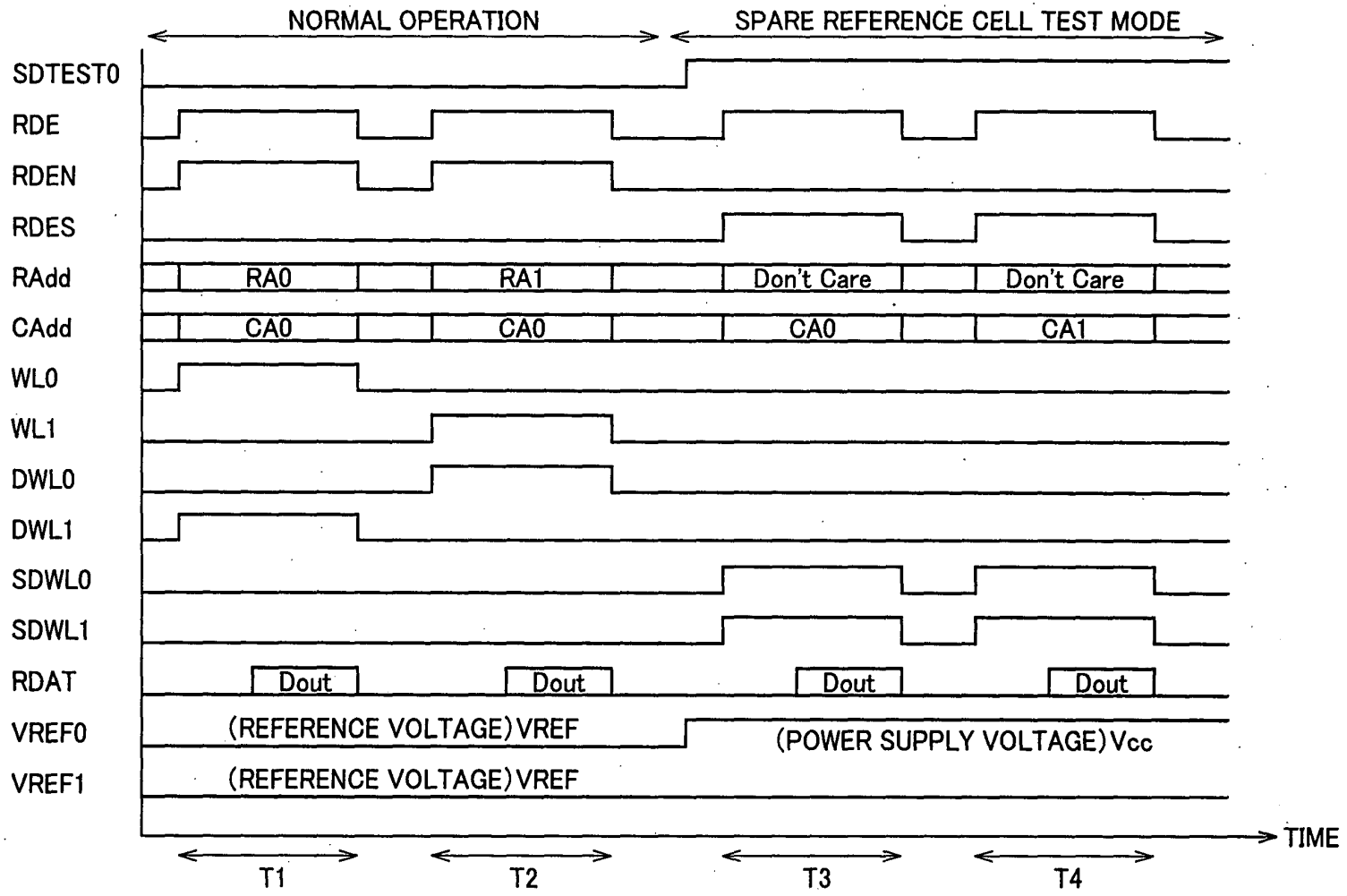

NORMAL OPERATION
SPARE REFERENCE CELL TEST MODE
SDTEST0
RDE
RDEN
RDES
RAdd
RA0
RA1
Don't Care
Don't Care
CAdd
CA0
CA0
CA0
CA1
WL0
WL1
DWL0
DWL1
SDWL0
SDWL1
RDAT
Dout
Dout
Dout
Dout
VREF0
(REFERENCE VOLTAGE)VREF
(POWER SUPPLY VOLTAGE)Vcc
VREF1
(REFERENCE VOLTAGE)VREF
TIME
T1
T2
T3
T4

FIG.17

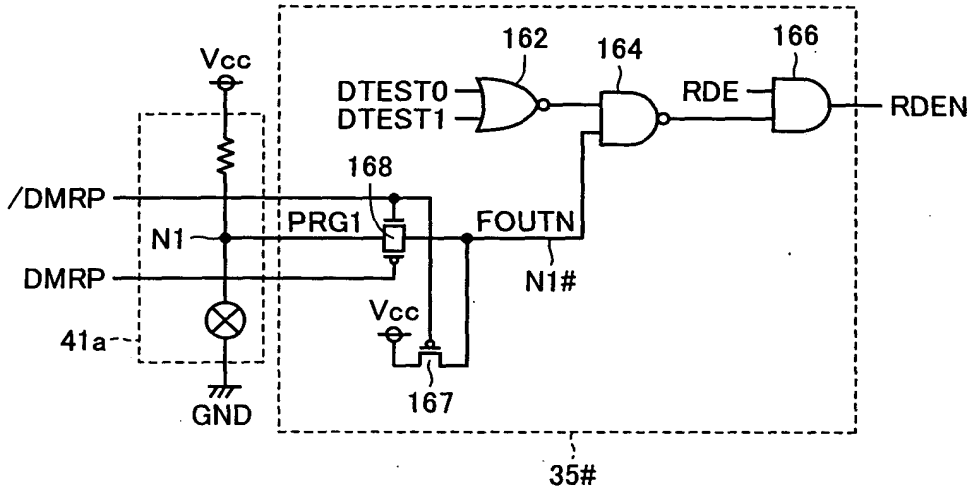

Vcc
162
164
166
DTEST0
DTEST1
RDE
RDEN
168
/DMRP
PRG1
FOUTN
N1
N1#
DMRP
Vcc
41a
167
GND
35#

FIG.18

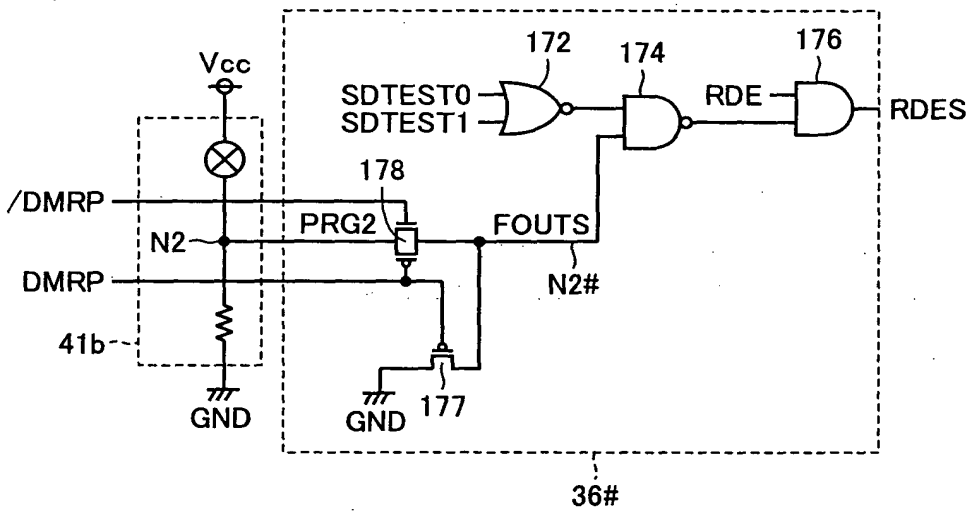

Vcc
172
174
176
SDTEST0
SDTEST1
RDE
RDES
178
/DMRP
PRG2
FOUTS
N2
N2#
DMRP
41b
GND
GND
177
36#

FIG.19

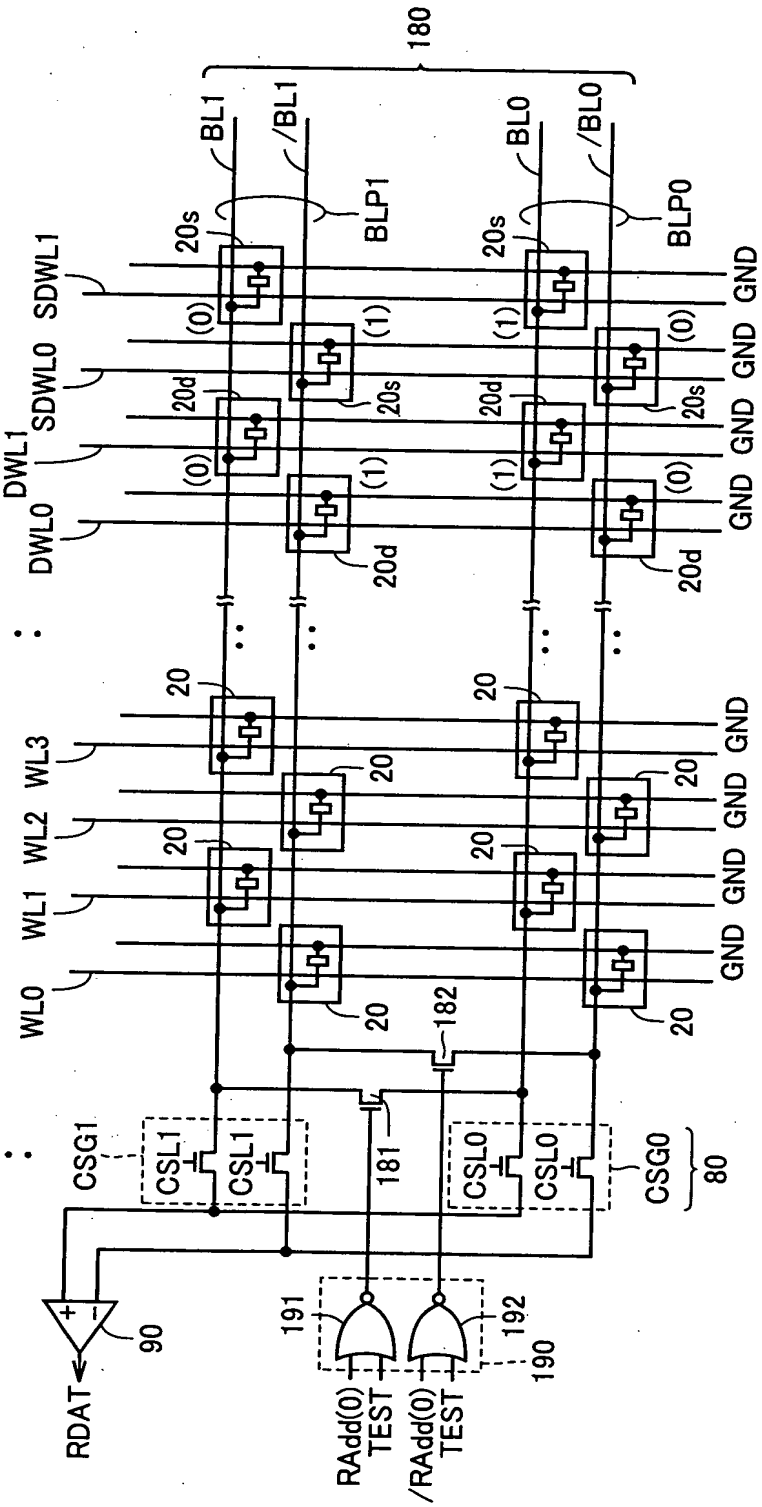

180
BL1
/BL1
BLP1
BL0
/BL0
BLP0
20s
20d
20
SDWL1
SDWL0
DWL1
DWL0
WL3
WL2
WL1
WL0
GND
CSG1
CSL1
CSG0
CSL0
80
181
182
191
192
190
90
RDAT
RAdd(0)
TEST
/RAdd(0)
TEST

FIG.20

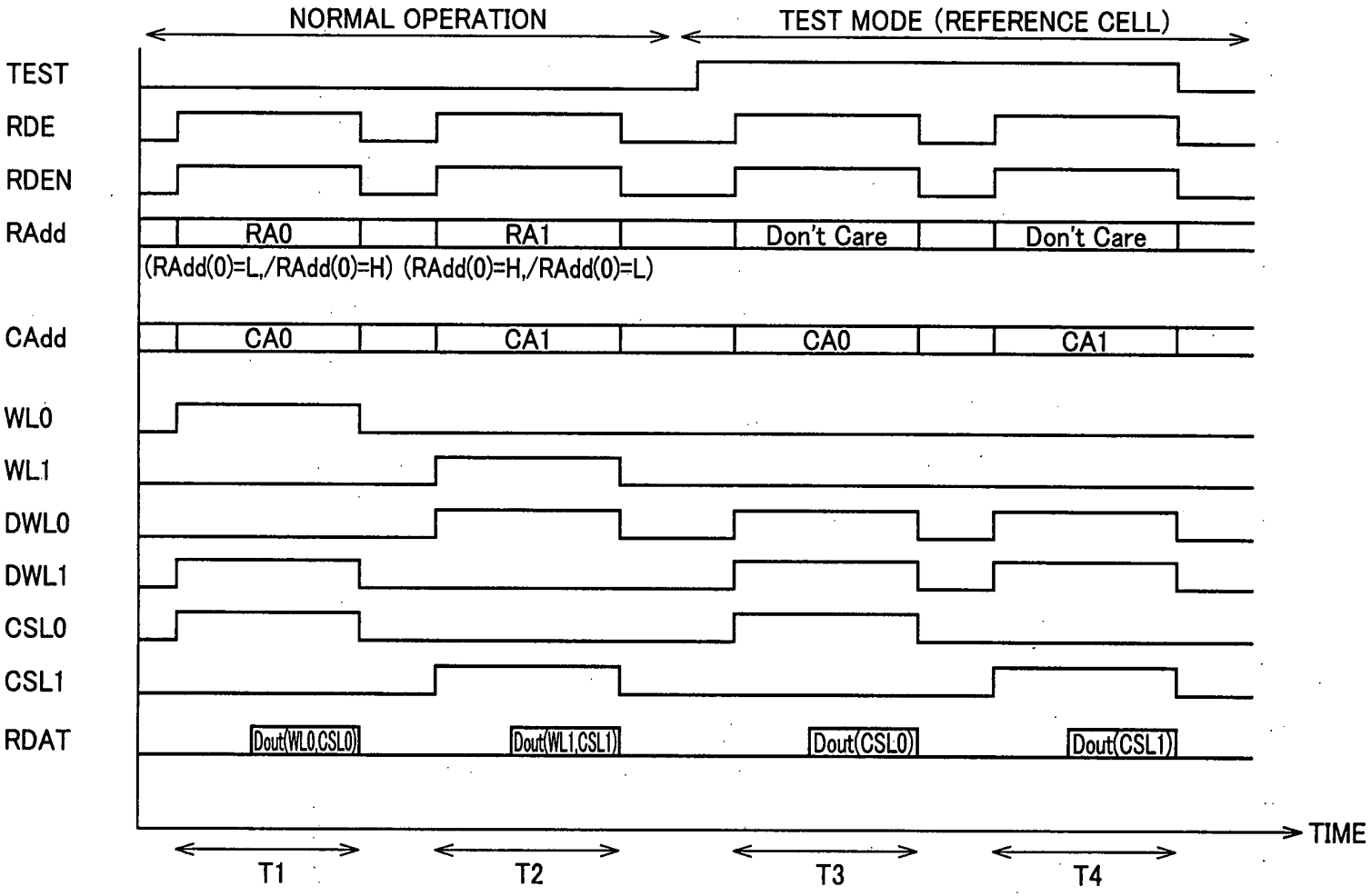

NORMAL OPERATION
TEST MODE (REFERENCE CELL)
TEST
RDE
RDEN
RAdd
RA0
RA1
Don't Care
Don't Care
(RAdd(0)=L,/RAdd(0)=H)
(RAdd(0)=H,/RAdd(0)=L)
CAdd
CA0
CA1
CA0
CA1
WL0
WL1
DWL0
DWL1
CSL0
CSL1
RDAT
Dout(WL0,CSL0)
Dout(WL1,CSL1)
Dout(CSL0)
Dout(CSL1)
TIME
T1
T2
T3
T4

FIG.21A

NO DEFECT (FOR BOTH REGULAR MEMORY CELL & REFERENCE MEMORY CELL)

RAdd(0)	WL0,2,4,6,···	WL1,3,5,···	DWL0	DWL1	SDWL0	SDWL1
0(L)	SELECT	NON-SELECT	NON-SELECT	SELECT	NON-SELECT	NON-SELECT
1(H)	NON-SELECT	SELECT	SELECT	NON-SELECT	NON-SELECT	NON-SELECT

FIG.21B

REPLACEMENT OF REGULAR MEMORY CELL (REGULAR WORD LINE)

RAdd(0)	WL0,2,4,6,···	WL1,3,5,···	DWL0	DWL1	SDWL0	SDWL1
0(L)	SELECT	NON-SELECT	NON-SELECT	SELECT	SELECT	NON-SELECT
1(H)	NON-SELECT	SELECT	SELECT	NON-SELECT	NON-SELECT	SELECT

(NON-SELECTION OF DEFECTIVE WL ONLY)

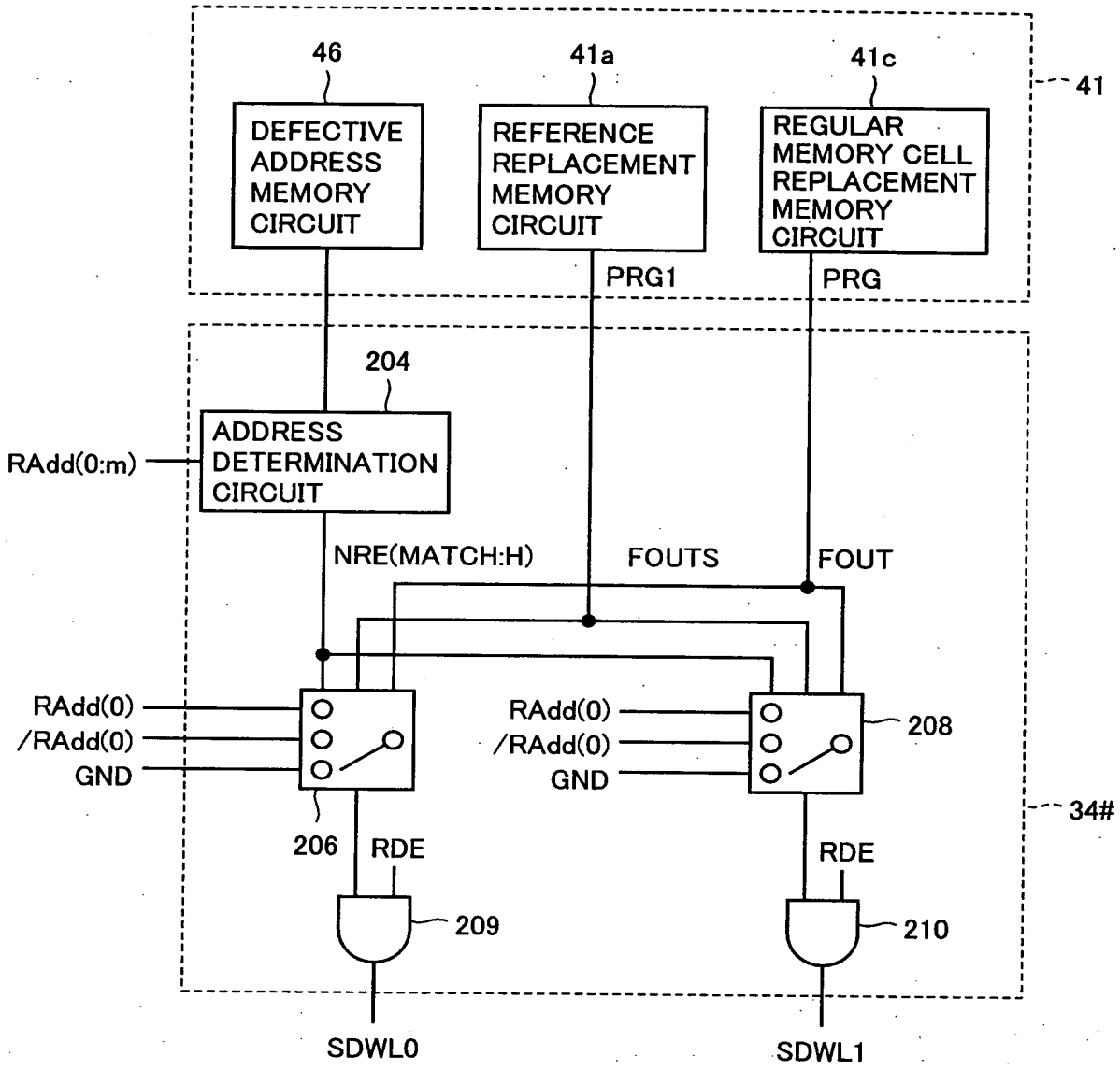
(ONLY WHEN DEFECTIVE WL IS SELECTED)

FIG.21C

REPLACEMENT OF REFERENCE CELL (DUMMY WORD LINE)

RAdd(0)	WL0,2,4,6,···	WL1,3,5,···	DWL0	DWL1	SDWL0	SDWL1
0(L)	SELECT	NON-SELECT	NON-SELECT	NON-SELECT	NON-SELECT	SELECT
1(H)	NON-SELECT	SELECT	NON-SELECT	NON-SELECT	SELECT	NON-SELECT

FIG.22


46
41a
41c
41
DEFECTIVE ADDRESS MEMORY CIRCUIT
REFERENCE REPLACEMENT MEMORY CIRCUIT
REGULAR MEMORY CELL REPLACEMENT MEMORY CIRCUIT
PRG1
PRG
204
ADDRESS DETERMINATION CIRCUIT
RAdd(0:m)
NRE(MATCH:H)
FOUTS
FOUT
RAdd(0)
/RAdd(0)
GND
RAdd(0)
/RAdd(0)
GND
208
206
RDE
RDE
209
210
34#
SDWL0
SDWL1